REMARKS

Claims 1-50 are pending in the application.

Claims 1-50 are rejected.

Claims 55-59 have been added to further define embodiments of the present invention.

Claims 51-54 have been canceled without prejudice or disclaimer in response to the Examiners restriction requirement.

In the Examiner interview it was agreed to cancel Claims 51-54 per Examiner's restriction requirement. No other action was agreed to in the Examiner interview.

The Applicants respectfully assert that the amendments to Claims 4, 6, 16, 29, 31, and 40 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

I. DRAWINGS

FIG. 6 has been amended to change Operand Mask 606 to Operand Mask Data 606 to more clearly distinguish between the data that defines a portion of the Quadword Operand and that portion of the Quadword that is under the Operand Mask itself.

The following addresses items 9-17 in this action:

Item 09 The Examiner states that the drawings must show every feature of the invention specified in the claims. The Examiner states that the apparatus of Claim 1, specifically, the plurality of addressable registers, first comparison circuit, second comparison circuit, and dispatch circuit must be shown or the feature(s) canceled

from the claim(s). Likewise, the Examiner states that the data processing system of Claim 24, specifically, the plurality of addressable registers, first comparison circuit, second comparison circuit, and dispatch circuit must be shown or the feature(s) canceled from the claim(s).

Plurality of addressable registers:

First it is important to indicate that the data processing system of Claim 24 contains a CPU that contains a Storage Reference Buffer (SRB). On page 33, lines 18-21 of the Specification it states "CPU 1310 in data processing system 1300 may employ a processor to manage Load and Stores using a SRB 212 operating according to embodiments of the present invention." Regarding the SRB 212, the Applicants offer the following from the Specification relative to the Detailed Description of FIG. 6 on page 9, lines 20-24 through page 12, line 22.

"FIG. 6 is a diagram illustrating the fields of an entry in the SRB 212. **Registers** of the SRB 212, according to embodiments of the present invention, **are addressed** by the use of pointers. Pointers contain the addresses of the registers in the SRB 212. Particular pointers, for example the IN pointer 615 and the OUT pointer 614 are loaded with particular register addresses which are indexed under certain conditions. The IN pointer 615 points to the register where a register entry is next added and OUT pointer 614 points to the register where a register entry is next retired or removed. If the SRB 212 has 64 register positions (0-63), both the IN pointer 615 and the OUT pointer 614 may point to an initial register address of 63. After the first register entry, the IN pointer 615 is decremented to 62 while the OUT pointer 614 remains with pointer value 63. When another register entry is added, the IN pointer 615 is again decremented to 61 and the OUT pointer 614 remains at 63. If the first entry (which contains a Load or a Store operation) completes, the OUT pointer is decremented to 62 and the IN pointer remains at 61. The SRB 212, in embodiments of the present invention is structured so the pointers roll over after they reach a zero to the maximum value (e.g., 63). In this manner the SRB 212 is a circular buffer.

The following details the organization of a register 600 in SRB 212. Valid bit (1 bit) 601 indicates the validity of the Quadword 607 during Loads and Stores. If an operation is a Load, the Quadword 607 becomes valid as soon as the full Quadword has been fetched. For a Store, the Quadword 607 becomes valid only if the Stored operand (1, 2, 4, or 8 bytes) becomes valid and the remaining bytes have been fetched from a valid location or from the cache. Instruction ID (6 bits) 602 is used to identify the instruction associated with a Load/Store. There may be more than one entry with the same instruction ID, as when multiple Quadwords are needed to satisfy a Load or a Store. In these cases, instructions with the same instruction ID will all be adjacent. Status (3 bits) 603 indicates the status of SRB 212 entries. Load/Store (1 bit) 604 indicates whether the operation is a Load or a Store. Real Address (64 bits) 605 refers to the Quadword real address which is needed before the D-cache 213 may be accessed. Operand Mask 606 is essentially a 16-bit field that indicates selected bytes in a Quadword. Although the Operand Mask 606 is 16 bits, not all states are valid. The operand mask is on 1, 2, 4, 8 byte boundaries. Quadword operands 607 are the 16 bytes of data accessed from a D-Cache line."

The preceding clearly describes that the SRB 212 is a circular buffer comprising a plurality of addressable registers, thus providing the support for these elements in Claim 1. Likewise, the data processing system 1300 has a CPU 1310 that may employ a SRB to manage Load and Store operations providing the support for plurality of addressable registers in Claim 24.

First comparison circuit:

In the Specification page 14, lines 23-23 through page 15, line 19 is the following.

"FIG. 11 is a state transition diagram further explaining a Load operation according to embodiments of the present invention. There are four states that a Load operation transitions starting when it "enters" the SRB 212 until it is completed and

"leaves" the SRB 212. EE 1106 indicates that the Load operation has established entry to SRB 212 by the Load Requested state 1101. After the Load Requested state 1101 a "filter", AA 1107, performs steps 1001, 1002 and 1003 of FIG. 10 and transitions to the Unresolved Load Request state 1102. Filters, according to embodiments of the present invention, are uniquely associated with each service (operations that are performed on data entry fields). All filters operate in parallel, checking to determine whether there is any **entry** that needs the particular service of the filter, selecting the earliest entry if there are several, and **dispatching** that **entry** to the hardware that performs the service[***dispatch circuit***]. The filters also perform the operation of "**scanning**" the entry fields of the SRB 212. Scanning may be done with a multiplexer or other circuit that allows a predetermined input value (e.g., a real address) to be **compared** to a value in like data entry fields [***first comparator circuit***](e.g. Real Address fields 605) in the SRB 212 registers to **determine a match**.

On a match, the **address of the register** containing the matching value is **compared** [***second comparator circuit***] to the register addresses bounded by register address pointers (e.g., IN pointer 615 and OUT pointer 614). Other operations may be done on data entry fields of a register corresponding to a matching value as a result of scanning based on a decode of other data entry fields (e.g. Instruction Status field 605)."

In this recitation it is clear that the SRB 212 has *a plurality of addressable registers, each of said registers partitioned into plurality of data entry fields*;

a first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value;

a second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address; and

a dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in

response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit.

The Applicants respectfully assert that clearly one of ordinary skill in the art understands from the detailed description of operations of the SRB cited above and other details in the Specification that these elements, while not specifically shown and designated as "plurality of registers", "first comparison circuit", "second comparison circuit", and "dispatch circuit", are contained in the SRB which is in turn contained in the SMU. Therefore, the Applicants respectfully assert that the objection of the drawings under 37 C.F.R. §1.83(a) are traversed.

Item 11 Please amend FIG 2 to change the TLB 203 in SMU 103 to TLB 223. The Specification is amended to conform to the drawing change. A new drawing for FIG 2 is included in this response. A new drawing for FIG 2 is included in this response.

Item 12 Please amend FIG 9 as follows. FIG.. 9 has been amended to add a couple of brackets to more clearly indicate what is Real Address 914 and what is Quadword 912. A new designator 916 was added that corresponds to the section of Quadword 912 pointed to by step 909 as "Operand Mask." Likewise, to avoid confusion section 915 was renamed "Operand Mask Data" from "Operand Mask." The Operand Mask Data 915 defines which portion of Quadword 912 is the "Operand" under the "Operand Mask 916" updated in step 909. A new drawing for FIG 9 is included in this response.

Item 13 Please amend FIG 10 as follows. FIG 10 has been amended to add a couple of brackets to more clearly indicated what is Real Address 1009 and what is Quadword 1010. A new designator 1012 was added that corresponds to the section of Quadword 1010 pointed to by step 1008. Likewise, to avoid confusion section 1011 was renamed "Operand Mask Data" from "Operand Mask." The Operand Mask Data 915

defines which portion of Quadword 1010 is the "Operand" under the "Operand Mask 1012" extracted in step 1008. A new drawing for FIG. 10 is included in this response.

Item 14 Please amend FIG. 13 by deleting element 1340 so FIG. 13 conforms to the Specification. The Specification has been amended to conform to the designators used for mouse 1326 and trackball 1332. A new drawing for FIG. 13 is included in this response.

Item 15 Please amend FIG. 9 as follows. FIG. 9 has been amended to add a couple of brackets to more clearly indicate that 912 is the Quadword and 911 is a portion of the Quadword under a complement Operand Mask. A new drawing for FIG. 9 is included in this response.

Item 16 Please amend FIG. 13 to add display 1338 so that the FIG. 13 conforms to the Specification. The Specification has been amended changing designator 1323 to 1332 to conform to FIG. 13. A new drawing for FIG. 13 is included in this response.

Item 17 Please amend the Specification to add the designator 503 to the description of the connection between IMU 102 and Data Aligner 502 so that the FIG. 5 and the Specification conform.

Please amend the Specification to add a description of designator 600. Descriptions of elements 620 is present on page 11 of the Specification. The Specification on page 11 has been amended to add designators 616-619 to their corresponding descriptions.

Element 912 is on page 16, line 15. Element 915 is found on page 13 line 6. However the description of element 915 had been amended to read "Operand Mask Data" to distinguish the portion of the Quadword under the Operand Mask and the data describing this portion.

The Specification is amended to add the designator 1011 to the description of that element.

The Specification is amended to add the description of element EE 1205.

FIG. 13 has been amended to drop element 1340 for which there is no description. The Specification is amended to change the designator 1323 to 1326 to make the Specification conform to FIG. 13.

II. REJECTION UNDER 35 U.S.C. § 112

The Examiner rejected Claims 1-50 under *35 U.S.C. §112* first paragraph as failing to comply with the enablement requirement. Likewise the Examiner rejected Claims 1-50 under *35 U.S.C. §112* second paragraph as failing to particular point out and distinctly claim the subject matter. In the case of *35 U.S.C. §112* first paragraph, the Examiner states that the limitations of Claim 1 and 26 are not described in such a way that they are enabled. In the case of *35 U.S.C. §112* second paragraph, the Examiner states that there is insufficient basis in the specification for the limitations in these claims. The following arguments will address both the *35 U.S.C. §112* first and second paragraph rejections.

Specifically, the Examiner states that Claims 1 and 26 recite the limitations of a first comparison circuit, a second comparison circuit, and a dispatch circuit. The Examiner stated that he could not locate in the Specification a clear and concise description of an apparatus which includes the first and second comparison circuits and dispatch circuit and operates them as described in the claim language.

The Examiner states that the apparatus of Claim 1, specifically the plurality of addressable registers, first comparison circuit, second comparison circuit, and dispatch circuit must be shown or the feature(s) canceled from the claim(s). Likewise, the Examiner states that the data processing system of Claim 26, specifically, the plurality

of addressable registers, first comparison circuit, second comparison circuit, and dispatch circuit must be shown or the feature(s) canceled from the claim(s).

Plurality of addressable registers:

First it is important to indicate that the data processing system contains a CPU that contains a Storage Reference Buffer (SRB). On page 33, lines 18-21 of the Specification it states "CPU 1310 in data processing system 1300 may employ a processor to manage Load and Stores using a SRB 212 operating according to embodiments of the present invention." Regarding the SRB 212 the Applicants offer the following from the Specification relative to Detailed Description of FIG. 6 on page 9, lines 20-24 through page 12, line 22.

"FIG. 6 is a diagram illustrating the fields of an entry in the SRB 212. **Registers** of the SRB 212, according to embodiments of the present invention, **are addressed** by the use of pointers. Pointers contain the addresses of the registers in the SRB 212. Particular pointers, for example the IN pointer 615 and the OUT pointer 614 are loaded with particular register addresses which are indexed under certain conditions. The IN pointer 615 points to the register where a register entry is next added and OUT pointer 614 points to the register where a register entry is next retired or removed. If the SRB 212 has 64 register positions (0-63), both the IN pointer 615 and the OUT pointer 614 may point to an initial register address of 63. After the first register entry, the IN pointer 615 is decremented to 62 while the OUT pointer 614 remains with pointer value 63. When another register entry is added, the IN pointer 615 is again decremented to 61 and the OUT pointer 614 remains at 63. If the first entry (which contains a Load or a Store operation) completes, the OUT pointer is decremented to 62 and the IN pointer remains at 61. The SRB 212, in embodiments of the present invention is structured so the pointers roll over after they reach a zero to the maximum value (e.g., 63). In this manner the SRB 212 is a circular buffer.

The following details the organization of a register 600 in SRB 212. Valid bit (1 bit) 601 indicates the validity of the Quadword 607 during Loads and Stores. If an operation is a Load, the Quadword 607 becomes valid as soon as the full Quadword has been fetched. For a Store, the Quadword 607 becomes valid only if the Stored operand (1, 2, 4, or 8 bytes) becomes valid and the remaining bytes have been fetched from a valid location or from the cache. Instruction ID (6 bits) 602 is used to identify the instruction associated with a Load/Store. There may be more than one entry with the same instruction ID, as when multiple Quadwords are needed to satisfy a Load or a Store. In these cases, instructions with the same instruction ID will all be adjacent. Status (3 bits) 603 indicates the status of SRB 212 entries. Load/Store (1 bit) 604 indicates whether the operation is a Load or a Store. Real Address (64 bits) 605 refers to the Quadword real address which is needed before the D-cache 213 may be accessed. Operand Mask 606 is essentially a 16-bit field that indicates selected bytes in a Quadword. Although the Operand Mask 606 is 16 bits, not all states are valid. The operand mask is on 1, 2, 4, 8 byte boundaries. Quadword operands 607 are the 16 bytes of data accessed from a D-Cache line."

The preceding clearly describes that the SRB 212 is a circular buffer comprising a plurality of addressable registers, thus providing the support for these elements in Claim 1. Likewise, the data processing system 1300 has a CPU 1310 that may employ a SRB to manage Load and Store operations providing the support for plurality of addressable registers in Claim 24.

First comparison circuit:

In the Specification page 14, lines 23-23 through page 15, line 19 is the following.

"FIG. 11 is a state transition diagram further explaining a Load operation according to embodiments of the present invention. There are four states that a Load operation transitions starting when it "enters" the SRB 212 until it is completed and

"leaves" the SRB 212. EE 1106 indicates that the Load operation has established entry to SRB 212 by the Load Requested state 1101. After the Load Requested state 1101 a "filter", AA 1107, performs steps 1001, 1002 and 1003 of FIG. 10 and transitions to the Unresolved Load Request state 1102. Filters, according to embodiments of the present invention, are uniquely associated with each service (operations that are performed on data entry fields). All filters operate in parallel, checking to determine whether there is any **entry** that needs the particular service of the filter, selecting the earliest entry if there are several, and **dispatching** that **entry** to the hardware [***dispatch circuit***] that performs the service. The filters also perform the operation of "**scanning**" the entry fields of the SRB 212. Scanning may be done with a multiplexer or other circuit that allows a predetermined input value (e.g., a real address) to be **compared** to a value in like data entry fields [***first comparator circuit***](e.g. Real Address fields 605) in the SRB 212 registers to **determine a match**.

On a match, the **address of the register** containing the matching value is **compared** [***second comparator circuit***] to the register addresses bounded by register address pointers (e.g., IN pointer 615 and OUT pointer 614). Other operations may be done on data entry fields of a register corresponding to a matching value as a result of scanning based on a decode of other data entry fields (e.g. Instruction Status field 605)."

In this recitation it is clear that the SRB 212 has *a plurality of addressable registers, each of said registers partitioned into plurality of data entry fields*;

a first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value;

a second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address; and

a dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in

response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit.

The Applicants respectfully assert that clearly one of ordinary skill in the art understands from the detailed description of operations of the SRB cited above and other details in the Specification that these elements, while not specifically shown and designated as "plurality of registers", "first comparison circuit", "second comparison circuit", and "dispatch circuit", are contained in the SRB which is in turn contained in the SMU.

Additionally the Applicants would point out the following from the Detailed Descriptions of Drawings in the Specification:

FIG. 1 and its detailed description on page 7, lines 14-20 discuss the operation of the SMU 103 (containing SRB 212) and IFU 101, IMU 102 and SMU 103.

FIG. 2 and its detailed description on page 7, lines 21-24 and page 8, lines 1-6 discuss that SMU 103 comprises SRB 212 and TLB 203 and other operations.

FIG. 3 and its detailed description on page 8, lines 6-14 discus operation of additional units with SMU 103 (with SRB 212) and ITL 305.

FIG. 4 and its detailed description on page 8, lines 15-22 discus operation of additional units and SMU 103 (with SRB 212) and IWB 204, IFU 101, and ATU 403.

FIG. 5 and its detailed description on page 8, lines 23-24 and page 9, lines 1-19 discuss operation of SRB 212 with IFU 101, IMU 102, DCU 501 and Data Aligner 502.

FIG. 6 and its detailed description on page 9, lines 20-24 through page 12, line 22 discuss details of the register structure of SRB 212.

These references and other details tie together the operation of the SRB 212 which contains a plurality of "addressable registers", a "first comparison circuit" for

scanning and comparing data entries in the register fields, "a second comparison circuit" for comparing addresses of the registers and the data fields, and a "dispatch circuit" for dispatching data from the register fields to other hardware units.

As further evidence the following if from the Summary of the Invention in the Specification of the present invention:

"A Storage Management Unit (SMU) comprises a Storage Reference Buffer (SRB) and Data Cache memory (D-Cache). The SRB comprises a set of contiguous registers accessed by the use of address pointers (pointers). The pointer operation is such that the SRB operates as a circular buffer where the content of pointers roll over from a maximum back to the minimum and vice versa depending on the indexing of the pointer. Register entries into the SRB are partitioned into data entry fields. These fields have data in the form of real addresses and Quadwords stored in memory space at these addresses as well as control information that determines what operations are applied to the data. The SRB is content addressed in that entries are tracked based on the real address data contained in a field of the entry. The SRB is used to manage Load and Store operations within the system. When the SMU receives a request for access to a real address, the real addresses is sent to D-Cache as well as to the SRB which acts as a small level zero (L0) cache ahead of the level one (L1) D-Cache. If the requested real address is found in the SRB and the control information indicates it is valid, the request to the D-Cache may be canceled, speeding up Load and Store operations. The SRB operates as a data flow architecture in that the control information associated with a particular real address is contained in the entry that also contains the real address. Several pointers are defined for the SRB indicating registers next in line to receive an entry, remove an entry, and defining windows or groups of registers in which a particular entry may be used for a current Load or Store operation. Operations on data entry fields of a SRB entry are processed using pipeline execution units. Data entry fields are scanned to determine content matches and operations are performed on selected data entry fields based on decode of other data entry fields and availability of processing resources.

As a result of the above arguments, the Applicants assert that the required support for Claims 1-50 is found in the Specification as filed. Therefore, the Applicants respectfully assert that the rejection of Claims 1-50 under *35 U.S.C. §112* first paragraph as failing to comply with the enablement requirement are traversed.

III. REJECTION UNDER 35 U.S.C. § 102(b)

The Examiner rejected Claims 1-12 and 14-25 under *35 U.S.C. §102(b)* as being taught by U.S. Patent No. 5,764,946 to *Tran et al.* (hereafter "*Tran*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 is directed to an apparatus for managing operations in a processor comprising four interrelated elements. Element 1 is a plurality of addressable registers, wherein each register is partitioned into plurality of data entry fields. Element 2 is a first comparison circuit operable to scan and compare a value in a set of the data entry fields (within the plurality of addressable registers) to a predetermined input value. Element 3 is a second comparison circuit operable to compare a first register address, corresponding to a comparison match of said first comparison circuit, to a second register address. When the first comparison circuit finds a value in the data entry fields that matches the predetermined input value there is a comparison match and a corresponding first register address results. The second comparison circuit (Element 3) then compares the first register address to a second register address. Element 4 is a dispatch circuit operable to dispatch data, of a second data entry field of a second register corresponding to the second register address, to an operation unit in response to a decode of data in a third data entry field of the second register and a comparison match of the second comparison circuit. The Applicants have shown that all of these elements are within the

Storage Reference Buffer (SRB) of the present invention which in turn resides in the Storage Management Unit (SMU).

The Examiner states that *Tran* teaches an apparatus for managing operations of a processor and cites *Tran* column 6, line 52 to column 7, line 14. In this recitation *Tran* is describing a block diagram of a superscalar microprocessor 200 including a branch prediction unit 220 employing a way prediction unit in accordance with the present invention. As illustrated in the embodiment of FIG. 1, superscalar microprocessor 200 includes a prefetch/predecode unit 202 and a branch prediction unit 220 coupled to an instruction cache 204. Instruction alignment unit 206 is coupled between instruction cache 204 and a plurality of decode units 208A-208F (referred to collectively as decode units 208). Each decode unit 208A-208F is coupled to a respective reservation station unit 210A-210F (referred collectively as reservation stations 210), and each reservation station 210A-210F is coupled to a respective functional unit 212A-212F (referred to collectively as functional units 212). Decode units 208, reservation stations 210, and functional units 212 are further coupled to a reorder buffer 216, a register file 218 and a load/store unit 222. A data cache 224 is finally shown coupled to load/store unit 222, and an MROM unit 209 is shown coupled to instruction alignment unit 206. Generally speaking, instruction cache 204 is a high speed cache memory provided to temporarily store instructions prior to their dispatch to decode units 208. In one embodiment, instruction cache 204 is configured to cache up to 32 kilobytes of instruction code organized in lines of 16 bytes each (where each byte consists of 8 bits). During operation, instruction code is provided to instruction cache 204 by prefetching code from a main memory (not shown) through prefetch/predecode unit 202.

The Applicant respectfully asserts that the Examiner has failed to point out which of these multiplicity of units making up super scalar microprocessor 200 he considers is the apparatus of Claim 1 of the present invention. Since the apparatus of Claim 1 comprises the four elements detailed above, it is important to know which of these units the Examiner considers the apparatus of Claim 1 so that the relationship of the four

elements as detailed in Claim 1 can be determined for the unit the Examiner believes teaches the invention. For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. The identical invention must be shown in as complete detail as is contained in the claim.

The Examiner states that *Tran* teaches Element 1 of Claim 1 and cites *Tran*, column 1, line 49 to column 2, line 25. For the *Tran* reference to read on Element 1 of Claim 1, then the particular apparatus of *Tran* that the Examiner believes is the apparatus of Claim 1 must comprise a plurality of addressable registers, wherein each of the plurality of addressable registers is partitioned into a plurality of data entry fields. This can only be true if one of the units cited by the Examiner as being the apparatus for managing the operations in a processor does in fact contain the Element 1 of Claim 1. *Tran* in the recitation of column 1, line 49 to column 2, line 25 is discussing how the memory in a superscalar microprocessor are accessed. Memory does not manage any operation of a processor save for how the information stored by the memory is interpreted by another unit. The Applicants fail to see the relevance of this cited art with regards to Element 1 of Claim 1 of the present invention. Nowhere in this reference is an apparatus for managing operations of a processor mentioned, wherein the apparatus has a plurality of registers partitioned into a plurality of data entry fields. The Examiner has taken two disjointed passages of *Tran*; a description of a block diagram of a superscalar microprocessor and a discussion of how a memory system within a superscalar microprocessor may be organized and accessed and somehow determined that they teach elements of Claim 1 directed to an apparatus for managing operations of a processor wherein the apparatus comprises a plurality of registers partitioned into data entry fields. The Applicant fails to see the connection.

The Examiner further states that *Tran* teaches Element 2 of Claim 1 and cites *Tran* column 77, lines 33-47; column (sic) 779, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 44; and Figure 46. For these references to read on Claim 1 they must teach an

apparatus for managing operations of a processor, wherein the apparatus comprises a plurality of addressable registers and a first comparison circuit, wherein each of the plurality of addressable registers is partitioned into a plurality of data entry fields and the first comparison circuit is operable to scan and compare a value in a set of the data entry fields in the plurality of addressable registers to a predetermined input value.

In the first reference, column 77, lines 33-47 *Tran* discusses operations of a line-oriented re-order buffer (LOROB). The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference column 79, lines 24-55, *Tran* discusses operations of the LOROB with the X86 instruction set. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference column 80, line 5 to column 81 line3, *Tran* discusses the dependency checking required for store operations according to the invention of *Tran*. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference column 101, lines 45-60, *Tran* discusses the current within line dependency checking unit. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference column 102, lines 17-59, *Tran* discusses the previous lines dependency checking operation performed by the LOROB. The Examiner has failed to

specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 38, *Tran* is showing a block diagram of the matrix dependency checking in the LOROB. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 38 was cited by the Examiner above. *Tran* is showing addresses being compared to pointers. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 39, *Tran* is showing a block diagram illustrating the dependency checking required for store operations according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 39 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 39, *Tran* is showing a block diagram illustrating the dependency checking required for store operations according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 39 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 40, *Tran* is showing a block diagram illustrating the dependency checking required for load operations according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG.

40 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 44, *Tran* is showing a block diagram illustrating the current within line checking unit according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 44 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

In the reference FIG. 46, *Tran* is showing a block diagram illustrating the previous lines checking operation performed by the LOROB according to his invention. Nowhere in this diagram is the invention of Claim 1 taught or suggested. The description of FIG. 46 was cited by the Examiner above. The Examiner has failed to specifically point out what he believes is Element 2 of Claim 1 of the present invention and where is the link showing the relationship of Element 2 to Element 1 and to the apparatus of Claim 1 for managing the operation of a processor.

The Examiner further states that *Tran* teaches Element 3 of Claim 1 and cites *Tran* column 77, lines 33-47; column (sic)779, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 44; and Figure 46. For these references to read on Claim 1 they must teach an apparatus for managing operations of a processor, wherein the apparatus comprises a plurality of addressable registers, a first comparison circuit and a second comparison circuit, wherein each of the plurality of addressable registers is partitioned into a plurality of data entry fields, the first comparison circuit is operable to scan and compare a value in a set of the data entry fields in the plurality of addressable registers to a predetermined input value and the second comparison circuit is operable to compare a first register address,

corresponding to a comparison match of the firs comparison circuit, to a second register address. The Examiner cites the same references of *Tran* as teaching Element 3 of Claim 1 as he cited for Element 2. Nowhere in these recitations is the invention of Claim 1 taught or suggested. Likewise, the Examiner has failed to specifically point out what he believes is Element 3 of Claim 1 of the present invention and where is the link showing the relationship of Element 3, Element 2, and Element 1 to the apparatus of Claim 1 for managing the operation of a processor in any of the cited references.

The Examiner further states that *Tran* teaches Element 4 of Claim 1 and cites *Tran*, column 106, line 35 to column 107, line 62; FIG 48 and FIG 49. FIG 48 is a block diagram of a reservation station and FIG 49 is a block diagram of the bus structure for the reservations stations according to the invention of *Tran*. In column 106, line 35 to column 107, line 62 *Tran* discusses the operation of the element of FIG 48 and FIG 49. Nowhere in this recitation is the invention of Claim 1 taught or suggested. Likewise, the Examiner has failed to specifically point out what he believes is Element 4 of Claim 1 of the present invention and where is the link showing the relationship of Element 4, Element 3, Element 2, and Element 1 to the apparatus of Claim 1 for managing the operation of a processor in any of the cited references.

Therefore, the Applicants assert that the Examiner has failed to make a prima facie case showing that *Tran* in fact teaches the invention of Claim 1 including Element 1-4 and their particular relationship recited in the limitations of Claim 1. The Examiner has found registers, comparison circuits, and dispatch circuits in the voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, however, the Examiner has failed to specifically point out which units of correspond to the elements of Claim 1. Therefore, the Applicants assert the rejection of Claim 1 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed.

Claim 2 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 2 adds the limitation that the operations managed by the apparatus of Claim 1 are Load and Store operations. The Examiner states the *Tran* teaches the invention of Claim

2 and cites *Tran* column 77, lines 33-47; column (sic)779, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40.

Nowhere in this recitation is the invention of Claim 2 taught or suggested. Likewise, the Examiner has failed to specifically point out what he believes is the limitation Claim 2 applied to the elements of Claim 1. Therefore, the Applicants assert that the Examiner has failed to make a prima facie case showing that *Tran* in fact teaches the invention of Claim 2 applied to Element 1-4 and their particular relationship recited in Claim 1. The Examiner found Load and Store operations in the voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1 wherein the units manage Load and Store operations. Therefore, the Applicants assert the rejection of Claim 2 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 3 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 3 adds the limitation that the predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation. The Examiner states the *Tran* teaches the invention of Claim 3 and cites *Tran* column 77, lines 33-47; column (sic)779, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40 which is the same reference as cited for Claim 1 and 2. The Examiner does not point out where to find the limitation of Claim 3 in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a prima facie case showing that *Tran* in fact teaches the invention of Claim 2 applied to Element 1-4 and their particular relationship recited in Claim 1. The Examiner found Load and Store operations in the voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, however, the Examiner has failed to specifically point out

which units of *Tran* correspond to the elements of Claim 1 wherein the units manage Load and Store operations and the predetermined input value of Claim 1 is a real address requesting particular data corresponding to one of the Load and Store operations. Therefore, the Applicants assert the rejection of Claim 3 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 4 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 4 adds the limitation that the first comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently and in parallel. The first comparison circuit of Claim 1 is operable to scan and compare a value in a set of the data entry fields in the plurality of registers to a predetermined input value. The Examiner states the *Tran* teaches the invention of Claim 4 and cites *Tran* column 77, lines 33-47; column (sic)779, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40 which is the same reference as cited for Claim 1-3. The Examiner does not specifically point out the limitation of Claim 4 in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a prima facie case showing that *Tran* in fact teaches the invention of Claim 4 applied to Element 1-4 and their particular relationship recited in Claim 1. The Examiner found comparators in the voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1 wherein the units manage Load and Store operations and the first comparator of Claim 1 is operable to scan and compare a value, in a set of said data entry fields in one of a plurality of addressable registers, each of said registers partitioned into plurality of data entry fields, to a predetermined input value and the first comparator circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently and in parallel. Therefore, the Applicants assert the rejection of Claim 4

under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 5 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 5 adds the limitation that the operation unit comprises an Instruction Management Unit (IMU). The Examiner states the *Tran* teaches the invention of Claim 5 and cites *Tran* column 77, lines 33-47; column (sic)779, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40 which is the same reference as cited for Claim 1-4 without specifically pointing out the limitation of Claim 5 in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a prima facie case showing that *Tran* in fact teaches the invention of Claim 5 applied to Element 1-4 and their particular relationship recited in Claim 1. The Examiner has made the statement that the limitation of Claim 5 is in voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1 wherein the management unit is an IMU. Therefore, the Applicants assert the rejection of Claim 5 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 6 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 6 adds the limitation that the operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB). The Examiner states the *Tran* teaches the invention of Claim 5 and cites *Tran* column 77, lines 33-47; column (sic)779, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40 which is the same reference as cited for Claims 1-5 without specifically pointing out where the limitation of Claim 6 is found in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a prima facie case showing that *Tran* in fact teaches the invention of Claim 6 applied to

Element 1-4 and their particular relationship recited in Claim 1. The Examiner has made the statement that the limitation of Claim 6 is in voluminous disclosure of *Tran* describing a superscalar microprocessor employing a way prediction unit, however, the Examiner has failed to specifically point out which units of *Tran* correspond to the elements of Claim 1 wherein comprises a Storage Management Unit (SMU) the SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB). Therefore, the Applicants assert the rejection of Claim 6 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 7 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 7 adds the limitation that the one of the data entry fields is a Valid bit field indicating whether other data entry fields are valid. The Examiner states the *Tran* teaches the invention of Claim 7 and cites *Tran* column 123, lines 2-15. While this recitation of *Tran* mentions that the "second field of the LOROB has the linear address and store data and the associated valid bits", it does not state what the valid bit indicate and specifically doe not state that the Valid bit field indicates whether other data entry fields are valid as recited in Claim 7 of the present invention. Therefore, the Applicants assert the rejection of Claim 7 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 8 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 8 adds the limitation that one of the data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation. The Examiner states the *Tran* teaches the invention of Claim 8 and cites *Tran* column 123, lines 2-15. The Applicants have shown that *Tran* does not teach the invention of Claim 1. Therefore *Tran* does not teach Claim 8 which further limits Claim 1. Therefore, the Applicants assert the rejection of Claim 8 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the same reasons as Claim 1.

Claim 9 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 9 adds the limitation that one of the data entry fields is an instruction status field corresponding to a status of one of the Load and Store operations. The Examiner states the *Tran* teaches the invention of Claim 8 and cites *Tran* column 123, lines 2-15. *Tran* does not mention an instruction status field in this reference and thus does not teach the limitation of Claim 9. The Applicants have shown that *Tran* does not teach the invention of Claim 1. Therefore, *Tran* does not teach Claim 9 which further limits Claim 1. Therefore, the Applicants assert the rejection of Claim 9 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the reasons above and for the same reasons as Claim 1.

Claim 10 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 10 adds the limitation that one of the data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state. The Examiner states the *Tran* teaches the invention of Claim 10 and cites *Tran* column 123, lines 2-15. In this recitation, *Tran* states that " each entry in the buffer is broken into three fields. The first field is made up of the LOROB instruction tag and the instruction type (load, store, or load-op-store)." It is clear that the first field comprises more than one bit. Claim 10 states that one of the data entry fields in the apparatus of Claim 1 is a Load/Store bit. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 1, therefore, *Tran* does not teach Claim 10 which further limits Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 10 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claim 1.

Claim 11 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 11 adds the limitation that one of the data entry fields comprises a Real Address field corresponding to a particular Real Address of memory data. The Examiner states the *Tran* teaches the invention of Claim 12 and cites *Tran* column 123, lines 2-15. In this

recitation, "the first field is made up of the LOROB instruction tag and the instruction type (load, store, or load-op-store). The second field has the linear address and store data and the associated valid bits, the update source being the functional units. The third field is made up of some control information (e.g., M bit indicating that this entry missed the data cache on a prior access, D bit indicating that the load in the entry is dependent on a store in the buffer), the update source being the load-store section itself." All of the fields in the LOROB of *Tran* are accounted for and none of them is described as comprising a Real Address field corresponding to a particular Real Address of memory data as recited in Claim 11 of the present invention. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 1, therefore, *Tran* does not teach Claim 11 which further limits Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 11 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claim 1.

Claim 12 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 12 adds the limitation that one of the data entry fields one of said data entry fields is a Quadword field comprising multiple bytes of data. The Examiner states the *Tran* teaches the invention of Claim 12 and cites *Tran* column 123, lines 2-15. In this recitation, "the first field is made up of the LOROB instruction tag and the instruction type (load, store, or load-op-store). The second field has the linear address and store data and the associated valid bits, the update source being the functional units. The third field is made up of some control information (e.g., M bit indicating that this entry missed the data cache on a prior access, D bit indicating that the load in the entry is dependent on a store in the buffer), the update source being the load-store section itself." All of the fields in the LOROB of *Tran* are accounted for and none of them is described as is a Quadword field comprising multiple bytes of as recited in Claim 12 of the present invention. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 1, therefore, *Tran* does not teach Claim 12 which further limits Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 12 under *35*

U.S.C. §102(b) as being taught by *Tran* is traversed for the above arguments and the same reasons as Claim 1.

Claim 14 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 14 adds the limitation that the operation unit is a pipeline execution unit operating concurrently on a plurality of the data entry fields. The Examiner states the *Tran* teaches the invention of Claim 14 and cites *Tran* column 10, lines 17-25 and FIG. 1. FIG. 1 of *Tran* is a block diagram of a superscalar microprocessor employing a branch prediction unit in accordance with the invention of *Tran*. See *Tran*, column 4, lines 32-34. Since a superscalar microprocessor is a CPU architecture that allows more than one instruction to be executed in one clock cycle, one of ordinary skill in the art would assume that *Tran* in FIG. 1 is showing the execution of multiple branch instructions in parallel. The Examiner has stated in his rejection of Claims 8-12 that he believes the data entry fields of Claim 1 are disclosed relative to the LOROB. FIG. 1 of *Tran* is not illustrating a pipeline execution unit operating concurrently on a plurality of the data entry fields of the LOROB of *Tran*. Therefore, the Applicants do not see the connection between the cited reference of *Tran* and Claim 14 of the present invention. The limitation of Claim 14 is relative to a specific apparatus as recited in Claim 1. FIG. 1 and column 10, lines 15-55 are describing branch prediction operations and functional units relative the superscalar microprocessor of *Tran*. The Applicants, respectfully assert that the Examiner must be consistent in his argument that a reference is disclosing inventive elements. The Examiner cannot assert that the data entry fields of Claim 1 are in the LOROB of *Tran* in one instance and then assert that parallel operations on branch instructions (FIG. 1 of *Tran*) teach a pipeline execution unit operating concurrently on a plurality of the same data entry fields (in LOROB). The Applicants have shown the data entry fields of the LOROB of *Tran* are not the data entry fields of Claim 1 of the present invention. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 1, therefore, *Tran* does not teach Claim 14 which further limits Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 14 under *35*

U.S.C. §102(b) as being taught by *Tran* is traversed for the above arguments and the same reasons as Claim 1.

Claim 15 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 15 adds the limitation that the addressable registers are addressed using a plurality of address pointers. The Examiner states the *Tran* teaches the invention of Claim 15 and cites *Tran* column 77, lines 33-47; column (sic)779, lines 24-55; column 80, line 5-column 81, line 3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; and Figure 40, which is the same reference as cited for Claims 1-5, without specifically pointing out where the limitation of Claim 15 is found in these multiple references of *Tran*. Therefore, the Applicants assert that the Examiner has failed to make a prima facie case showing that *Tran* in fact teaches the invention of Claim 15 applied to Element 1-4 and their particular relationship recited in Claim 1. Therefore, the Applicants assert the rejection of Claim 15 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claim 1.

Claim 16 is amended to correctly depend from Claim 6 where the SRB is first introduced. Amended Claim 16 depends from Claim 6 and contains all the limitations of Claim 6. Claim 16 adds the limitation that the addressable registers of Claim 1 are configured as the Storage Reference Buffer (SRB). The Examiner states the *Tran* teaches the invention of Claim 16 and cites *Tran* column 10, line 66 to column 11, line 15, column 77, lines 33-47; column (sic)779, lines 24-55; column 80, line 5-column 81, line 3; Figure 1, Figure 38; Figure 39; and Figure 40 without specifically pointing out where the limitation of Claim 16 is found in these multiple references of *Tran*. The Examiner does not specifically point out the limitation of Claim 16 in these multiple references of *Tran*, therefore, the Applicants assert that the Examiner has failed to make a prima facie case showing that *Tran* in fact teaches the invention of Claim 16 applied to Element 1-4 and their particular relationship recited in Claims 1 and 6. Therefore, the Applicants assert the rejection of Claim 16 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above reasons and for the same reasons as Claims 1 and 6.

Claim 17 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 17 adds the limitation that one of the address pointers is a third pointer pointing to one of the addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation. The Examiner states that *Tran* teaches the invention of Claim 17 and cites *Tran* column 70, lines 7-44 and FIG 36. FIG 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In this recitation *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein one of the address pointers is a third pointer pointing to one of the addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation. as recited in Claim 17. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 17 which further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 17 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 18 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 18 adds the limitation that the address pointers comprise a fourth and fifth pointer defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage. The Examiner states that *Tran* teaches the invention of Claim 18 and cites *Tran* column 70, lines 7-44 and FIG 36. FIG 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the address pointers comprise a fourth and fifth pointer defining a window of register addresses from

which a Load operation may be satisfied without having to access other memory storage as recited in Claim 18. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 18 which further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 18 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 19 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 19 adds the limitation that the second register address is selected from registers addresses which fall within a window of register addresses defined by the address pointers. The Examiner states that *Tran* teaches the invention of Claim 19 and cites *Tran* column 70, lines 7-44; column 81, lines 1-3 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the second register address is selected from registers addresses which fall within a window of register addresses defined by the address pointers as recited in Claim 19. In column 80, lines 1-3, *Tran* discloses that (sic) "the LOROB must partially retire the line until all entries with the load-match bits. The WRPTR signal indicates the load instructions can be executed." Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the second register address is selected from registers addresses which fall within a window of register addresses defined by the address pointers as recited in Claim 19. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 19 which further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 19 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 20 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 20 adds the limitation that one of the address pointers is a first pointer pointing to an IN register address of a first available register into which data may be added. The Examiner states that *Tran* teaches the invention of Claim 20 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein one of the address pointers is a first pointer pointing to an IN register address of a first available register into which data may be added as recited in Claim 20 . Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 20 which further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 20 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 21 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 21 adds the limitation that one of said address pointers is a second pointer pointing to an OUT register address of a first available register from which register data may be retired. The Examiner states that *Tran* teaches the invention of Claim 21 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein one of said address pointers is a second pointer pointing to an OUT register address of a first available register from which register data may be retired as recited in Claim 21. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 15, therefore, *Tran* does not teach Claim 21 which

further limits Claim 15. Therefore, the Applicants respectfully assert that the rejection of Claim 21 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 15.

Claim 22 is dependent from Claim 16 and contains all the limitations of Claim 15. Claim 22 adds the limitation that the data entry fields, added to the SRB after a mis-predicted branch instruction occurs in said processor, are retired and the first pointer is indexed to a first register address of a register with added register data entry bits which were added immediately prior to the mis-predicted branch instruction. The Examiner states that *Tran* teaches the invention of Claim 22 and cites *Tran* column 82, lines 63 to column 83, line 22. In column 82, lines 63 to column 83, line 22, *Tran* discloses that mis-prediction of branches are handled by the LOROB. *Tran* then describes what happens in his LOROB in response to the two types of branches. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the data entry fields, added to the SRB after a mis-predicted branch instruction occurs in said processor, are retired and the first pointer is indexed to a first register address of a register with added register data entry bits which were added immediately prior to the mis-predicted branch instruction as recited in Claim 22. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 16, therefore, *Tran* does not teach Claim 22 which further limits Claim 16. Therefore, the Applicants respectfully assert that the rejection of Claim 22 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 16.

Claim 23 is dependent from Claim 19 and contains all the limitations of Claim 19. Claim 23 adds the limitation that the window of register addresses defines active Load and Store operations. The Examiner states that *Tran* teaches the invention of Claim 23 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer

that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the second register address is selected from registers addresses which fall within a window of register addresses defined by the address pointers and the window of register addresses defines active Load and Store operations as recited in Claim 23. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 19, therefore, *Tran* does not teach Claim 23 which further limits Claim 19. Therefore, the Applicants respectfully assert that the rejection of Claim 23 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 19.

Claim 24 is dependent from Claim 20 and contains all the limitations of Claim 20. Claim 24 adds the limitation that the first pointer is indexed by one when the register data has been added and the first pointer has a minimum and a maximum value wherein a decrement down from a minimum value results in the maximum value and an increment up from the maximum value results in the minimum value. The Examiner states that *Tran* teaches the invention of Claim 24 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the first pointer is indexed by one when the register data has been added and the first pointer has a minimum and a maximum value wherein a decrement down from a minimum value results in the maximum value and an increment up from the maximum value results in the minimum value as recited in Claim 24. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 20, therefore, *Tran* does not teach Claim 24 which further limits Claim 20. Therefore, the Applicants respectfully assert that the rejection of Claim 24 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 20.

Claim 25 is dependent from Claim 21 and contains all the limitations of Claim 21 . Claim 25 adds the limitation that the second pointer is indexed by one when register entry bits have been deleted and the second pointer has a minimum and a maximum value wherein a decrement down from the minimum value results in the maximum value and an increment up from the maximum value results in the minimum value. The Examiner states that *Tran* teaches the invention of Claim 25 and cites *Tran* column 70, lines 7-44 and FIG. 36. FIG. 36 is a block diagram showing how the LOROB interfaces with other processor 500 units. See *Tran*, column 5, lines 47-48. In column 70, lines 7-44, *Tran* discloses that the LOROB has a single line pointer that has two 3 bit parts for a total of 6 bits. Nowhere in this reference does *Tran* mention or describe an apparatus as recited in Claim 1 with a plurality of address registers addressable by address pointers wherein the second pointer is indexed by one when register entry bits have been deleted and the second pointer has a minimum and a maximum value wherein a decrement down from the minimum value results in the maximum value and an increment up from the maximum value results in the minimum value as recited in Claim 24. Further, the Applicants have shown that *Tran* does not teach the invention of Claim 21, therefore, *Tran* does not teach Claim 24 which further limits Claim 21 . Therefore, the Applicants respectfully assert that the rejection of Claim 24 under *35 U.S.C. §102(b)* as being taught by *Tran* is traversed for the above arguments and the same reasons as Claims 1 and 21.

IV. REJECTION UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claim 13 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Jerry M. Rosenberg's* Dictionary of Computers, Information Processing &Telecommunications Second Edition © 1987 (herein referred to as *Rosenberg*).

The Examiner rejected Claims 26-37 and 19-50 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Kenneth L Short's* Microprocessors and Programmed Logic © 1981 (herein referred to as *Short*).

The Examiner rejected Claims 38 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Rosenberg* and further in view of *Short*.

To establish a *prima facie* case of obviousness, the Examiner must meet three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.

Claim 13 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 13 adds the limitation that one of the data entry fields is an Operand Mask field defining selected bytes of data within a selected one of the data entry fields. The Examiner states that *Tran* does not explicitly teach the invention of Claim 13. However, the Examiner states that *Tran* does teach miscellaneous control fields. The Applicants assert that it is not enough for *Tran* to teach miscellaneous control fields for *Tran* to read on Claim 13 of the present invention. Claim 13 only adds a limitation to the apparatus of Claim 1. The Applicants have shown that *Tran* does not teach or disclose an apparatus comprising four elements for managing operations in a processor with the relationship described in Claim 1, wherein addition one of the data entry fields is an Operand Mask

field defining selected bytes of data within a selected one of the data entry fields. Claim 1 is not reciting just any mask field (*Rosenberg* is simply presenting the definition of a mask field), rather Claim 1 is directed to particular data entry fields in the registers of the apparatus of Claim 1. An "operand" is the part of a machine instruction that references data. For example, in the instruction, "ADD A to B", A and B are the operands (nouns), and ADD is the operation code (verb). Therefore the Operand Mask field of Claim 13 refers to a particular mask that is one of the plurality of data entry fields in each of the plurality of addressable registers in the apparatus of Claim 1. In turn, the Operand Mask field of Claim 13 defines selected bytes of data within a selected one of the data entry fields of the addressable registers. *Rosenberg* adds nothing to the disclosure of *Tran* because *Tran* does not disclose that his control information is used to define selected bytes of data within a selected one of data entry fields of addressable registers in the apparatus of Claim 1. One of ordinary skill in the art would not look to *Rosenberg* to determine the function to apply to the control bits of *Tran*. The invention of Claim 13 could only be arrived at by combining *Tran* and *Rosenberg* using hindsight in view of the present invention. Simply knowing that *Tran* uses control bits and having *Rosenberg*'s definition of a mask field does not lead one of ordinary skill in the art to the invention of Claim 13. Therefore, the Applicants respectfully assert that the rejection of Claim 13 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Rosenberg* is traversed for the above arguments and for the same reasons as Claims 1.

Claim 26 is an independent claim directed to a data processing system that comprises a number of units including a processor that the apparatus with the limitations of Claim 1. The Applicants have shown that *Tran* does not teach or disclose the apparatus of Claim 1. The Examiner states that *Tran* teaches a data processing system comprising a CPU wherein the CPU includes the apparatus of Claim 1. *Tran* teaches a superscalar microprocessor, the Applicants have shown that *Tran* does not teach or disclose the apparatus of Claim 1 within this superscalar microprocessor, hence *Tran* does not teach the invention of Claim 26. The Examiner states the *Tran* does not teach a microprocessor comprising RAM, ROM, an I/O adapter, and a bus system coupling

devices internal to the CPU. However, the Examiner states that *Short* teaches a microprocessor comprising RAM, ROM, an I/O adapter, and a bus system coupling devices internal to the CPU. What is important is that *Short* does not teach or suggest a CPU the includes the apparatus of Claim 1. In fact, *Short* does not teach RAM and does not teach a bus system coupling devices internal to the CPU. *Short* is only used to show the general architecture of a microprocessor not included in the microprocessor of *Tran*. *Short* adds no teaching or suggestion that his defined microprocessor has a CPU with the apparatus of Claim 1. The Applicants respectfully assert that *Tran* and *Short* singly or in combination, do not teach or suggest the apparatus of Claim 1. Therefore, the Applicants assert that the rejection of Claim 26 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Rosenberg* is traversed for the above arguments and for the same reasons as Claim 1.

Claims 27-50 add the same limitations to Claim 26 and intervening claims as Claims 2-25 add to Claim 1 and intervening claims. The Examiner has rejected Claims 27-50 for the same reasons he has rejected Claims 2-25 with the exception that he relies on the teachings of *Short* for the units in the CPU of Claim 26 not disclosed by *Tran*. The Applicants have shown that *Short* adds nothing to the teachings of *Tran* relative to the apparatus of Claim 1. Therefore the Applicants respectfully assert that the rejections of Claims 27-50 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Rosenberg* are traversed for the above arguments and for the same reasons as Claim 2-25.

V. CONCLUSION

FIGS. 2, 6, 7, 10, and 13 have been amended as suggested by the Examiner and to more clearly conform to the Specification.

The Specification has been amended as suggested by the Examiner and to conform to the Drawings.

Claims 4, 6, 16, 29, 31 and 41 have been amended to correct informalities.

New dependent Claims 55-59 have been added.

The Applicants have traversed the rejections of Claims 1-50 under *35 U.S.C. §112* first paragraph as failing to comply with the enablement requirement. Likewise the Applicants have traversed the rejections of Claims 1-50 under *35 U.S.C. §112* second paragraph as failing to have sufficient basis in the Specification.

The Applicants have traversed the rejections of Claims 1-12 and 14-25 under *35 U.S.C. §102(b)* as being anticipated by *Tran*.

The Applicants have traversed the rejections of Claims 13, 26-37, and 19-50 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Short*.

The Applicants have traversed the rejections of Claim 38 under *35 U.S.C. §103(a)* as being unpatentable over *Tran* in view of *Short* further in view of *Rosenberg*.

The Applicants, therefore, respectfully assert that Claims 1-50 and new Claims 55-59 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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